REMARKS

Claims 1-21, all the claims pending in the application, stand rejected on prior art grounds. Claims 1, 6, 12, and 17 are amended herein. Moreover, new formal drawings are submitted herewith to provide enhanced clarity of the claimed invention. Applicants respectfully traverse the prior art rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-10 and 12-16 stand rejected under 35 U.S.C. §102(b) as being anticipated by Raghavan et al. (U.S. Patent No. 5,896,300), hereinafter referred to as "Raghavan". Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Darden et al. (U.S. Patent No. 6,185,722), hereinafter referred to as "Darden". Claims 17-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Raghavan in view of Darden and further in view of Chang et al. (U.S. Patent No. 5,901,063), hereinafter referred to as "Chang". Applicants respectfully traverse these rejections based on the following discussion.

Raghavan teaches a method, apparatus and computer program product performing a bounded parasitic extraction of typically all nets in an integrated circuit as part of a series of post-layout verification operations. According to one embodiment, a resistance-only extraction and/or a capacitance-only extraction is initially performed using computationally inexpensive electrical models of the nets. The resistance and capacitance extractions may be combined with models of the active devices to generate realistic worst case and best case delay models for each of the extracted nets. The delay models may be based on the resistance-only extraction and an upper bound on the parasitic capacitance of the net determined from the capacitance-only extraction,

however, other models based solely on a resistance-only extraction may also be used, although they are typically less preferred. A user-specified timing error tolerance is then used to automatically determine the appropriate level of additional extraction detail to be applied to the specific nets in the integrated circuit. This gives the user direct error control over the extraction process so that the extracted netlist meets the user-specified timing error tolerance in an efficient manner.

Darden teaches a computerized tool or method that calculates the capacitance and resistance of each global wire on the chip, one wire at a time. The invention steps along a track containing a wire segment, grid point by grid point, calculating the resistance and capacitance at that point. At each grid point it searches the neighboring tracks within the surrounding cube for adjacent elements that could cause capacitive effects or affect the resistance of the wire. The method delivers capacitance and resistance values for each process condition for a grid unit length of wire, given the wire type and 3 dimensional environment of the wire segment. The capacitance and resistance at a grid point along the wire are generally determined by one table lookup for wire types based on the surrounding environment. These values are added along wire segments to deliver accurate 3 dimensional capacitances and resistances. The invention can also provide for wires and spaces of various types and widths not provided for in the tables and for calculation of net to net coupling capacitances.

Chang teaches a comprehensive system and method allowing an integrated circuit designer to extract accurate estimates of parasitic impedances in interconnection lines of an integrated circuit. The method includes collecting values of electrical characteristic parameters to provide a technology profile for a particular fabrication process. An Interconnect Primitive

Library builder provides a collection of interconnect `primitives` that any interconnect structure fabricated under the fabrication process can be broken down into, and combines it with the technology profile for simulations in a 3-dimensional field solver to extract parameterized coupling capacitances and other characteristic impedances for each interconnect primitive. An extraction tool traces a signal path of an integrated circuit and decomposes the interconnect structures on the signal path into interconnect primitives and maps them to the Interconnect Primitive Library. An RC network module provides an RC network based on the characterized parametric values in the mapped interconnect primitives. The RC network thus provided can be used to accurately estimate signal delays in a circuit simulator or delay calculator.

As amended independent claims 1, 6, 12, and 17 contain features, which are patentably distinguishable from the prior art references of record. Specifically, the claims 1 and 12 recite, in part, "...extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions; extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions; determining a difference between said first cell characteristics and said second cell characteristics; labeling a placeability of said portion of said circuit design based on said difference; replacing said portion of said circuit with a leaf cell if said portion of said circuit design is freely placeable; and merging all overlapping shapes within said leaf cell into a single shape." Similarly, claim 6 recites, in part, "...merging all overlapping shapes within said placeholder cell into a single shape." Likewise, claim 17 recites, in part, "simplifying said placeholder cell by merging all overlapping shapes within said placeholder cell into a single shape, wherein said merging comprises...."

These features are simply not taught or suggested in the prior art references of record.

Another distinction of the claimed invention compared with the prior art references is that the claimed invention provides the impedance information on each port within the hierarchy. The parent cell port impedance contains everything within the parent cell, the impedances from the lower cell ports, and the extracted values from the connection to the parent cell. Another novel aspect of the claimed invention is that it calculates the impact of the changing environments. According to the claimed invention, the extraction methodology occurs for best case, average case, and worst case process conditions. Another novel aspect of the claimed invention is that it calculates the maximum change that can be caused by different placements. Thus, according to the claimed invention, the worst case environment includes the worst case process conditions, which includes all possible and properly spaced wire placements with actual wires. Nothing is added in the best case processes. The change in capacitance due to the additional wiring is then compared with the best case environment, which allows the ability to decide whether the cell performance is independent of the placement.

Then, according to the invention, the placeholder cell is created. The placeholder cell is simplified to deliver only the necessary information to the parent cell. The claimed invention simplifies the placeholder cell by shorting all conductors of the cell to a new common cell node, which is tied to ground. Conductors of the parent cell are still connected to the conductors of the cell, so their capacitance is not changed. Moreover, all conductors on the same physical level are merged into one shape, and any conductor covered by a higher or outside conductor is removed, thereby making the cell more simplified or "hollow". Because all conductors are on the same node, and fringe capacitances effectively enlarge any conductor to the outside, any close conductors can be merged into one shape, thereby removing holes out of the outside shell of the

placeholder to further simplify the placeholder cell. These steps significantly simplify the capacitance calculation from the parent to the placeholder cell, and deliver a significantly improved performance boost to the extraction step.

Additionally, the claimed invention is also more flexible than conventional programs and systems, such as those described in the prior art references, wherein the claimed invention evaluates the error according to the circuit needs. Moreover, the claimed invention delivers many more cases in which hierarchy can be used, and in this way, provides a much larger performance advantage than the prior art approaches.

The Office Action argues that claims 1-10 and 12-16 are completely anticipated by Raghavan. However, there are several noteworthy distinctions between the claimed invention and Raghavan. For example, Raghavan uses fast estimates to establish upper and lower bounds of the expected extraction results. Moreover, Raghavan then uses these values to establish whether further extraction is needed. However, Raghavan does not discuss hierarchy at all. Conversely, the claimed invention performs several functions that Raghavan does not.

For example, the claimed invention extracts a leaf cell in both optimistic and pessimistic environments to establish placeability, whether the cell needs to be extracted only once, and whether the extraction is accurate enough for any placement. Accordingly, there are two main differences between the claimed invention and Raghavan. First, the claimed invention does not vary the accuracy of the extraction method; it simply varies all possible geometric environments of the hierarchical block. Second, the claimed invention does not determine whether more accurate work is needed, but instead, whether the placement is free. These differences are significant in the distinction between the claimed invention and Raghavan.

Similarly, Darden is patentably distinguishable from the claimed invention. The claimed invention describes how to create a simplified block so that the extraction of the next higher cell in the hierarchy does not have to take into account (anticipate) the details of each placed leaf cell. The idea in the claimed invention is the removal of net detail, the merger of close structures, and the removal of invisible structures. In Darden blockages are disclosed to be used like metal in the global extraction. The Office Action equates these blockages with the placeholder (leaf) cell of the claimed invention. However, these are not the same. Moreover, the claimed invention does not involve how to create these blockages. Thus, the two inventions are not analogous.

Chang is also contrary to the claimed invention. For example, Chang discusses the use of pre-characterized environments for small wire segments to simplify a full 3D field calculation. However, Chang also does not address hierarchy, nor the details of the placeholder generation and its application to replace a placeable hierarchy level with a simplified view as does the claimed invention.

Insofar as references may be combined to teach a particular invention, and the proposed combination of Raghavan, Darden, and Chang in various combinations with one another, case law establishes that, before any prior-art references may be validly combined for use in a prior-art 35 U.S.C. § 103(a) rejection, the individual references themselves or corresponding prior art must suggest that they be combined.

For example, in In re Sernaker, 217 U.S.P.Q. 1, 6 (C.A.F.C. 1983), the court stated: "[P]rior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings." Furthermore, the court in Uniroyal, Inc. v. Rudkin-Wiley Corp., 5 U.S.P.Q.2d 1434 (C.A.F.C.

1988), stated, "[w]here prior-art references require selective combination by the court to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself. . . . Something in the prior art must suggest the desirability and thus the obviousness of making the combination."

In the present application, the reason given to support the proposed combination is improper, and is not sufficient to selectively and gratuitously substitute parts of one reference for a part of another reference in order to try to meet, but failing nonetheless, the Applicant's novel claimed invention. Furthermore, the claimed invention, as amended, meets the above-cited tests for obviousness by including embodiments such as merging all overlapping shapes within the placeholder (leaf) cell into a single shape, as generally recited in amended claims 1, 6, 12, and 17. As such, all of the claims of this application are, therefore, clearly in condition for allowance, and it is respectfully requested that the Examiner pass these claims to allowance and issue.

As declared by the Federal Circuit:

> In proceedings before the U.S. Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992) citing In re Fine, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988).

Here, the Examiner has not met the burden of establishing a prima facie case of obviousness. It is clear that, not only does Raghavan fail to disclose all of the elements of the claims of the claimed invention, particularly merging all overlapping shapes within the

placeholder (leaf) cell into a single shape, as discussed above, but also, if combined with Darden and Chang, fails to disclose this element as well. The unique elements of the claimed invention are clearly an advance over the prior art.

The Federal Circuit also went on to state:

> The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. . . . Here the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. Fritch at 1784-85, citing In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

Here, there is no suggestion that Raghavan, alone or in combination with Darden and/or Chang teaches a structure containing all of the limitations of the claimed invention. Consequently, there is absent the "suggestion" or "objective teaching" that would have to be made before there could be established the legally requisite "prima facie case of obviousness."

Additionally, clearly the invention is part of a crowded art field. As such, given the crowdedness of the art, the novel aspects of the invention should be regarded as a significant step forward in the constant development of this technical art field. Furthermore, the invention clearly provides for a vastly superior performing method and design compared to the prior art approaches.

In view of the foregoing, the Applicant respectfully submits that the collective cited prior art do not teach or suggest the features defined by amended independent claims 1, 6, 12, and 17 and as such, claims 1, 6, 12, and 17 are patentable over Raghavan alone or in combination with

either Darden or Chang. Further, dependent claims 2-5, 7-11, 13-16, and 18-21 are similarly patentable over Raghavan alone or in combination with either Darden or Chang, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Thus, the Applicant respectfully requests that these rejections be reconsidered and withdrawn.

Moreover, the Applicant notes that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

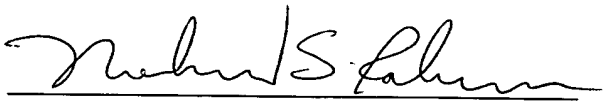
In view of the foregoing, Applicants submit that claims 1-21, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: December 11, 2003



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